REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-11. Specifically, the Office Action rejected claims 1 and 6 under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement. The Office Action further rejected claim 1-11 under 35 U.S.C. 102(b) as being anticipated by Crouch (U.S. Patent No.5,592,493, "Crouch" hereinafter). Applicants have amended claims 1-3, 5-8 and 10 and canceled claims 4 and 9. After entry of the foregoing amendments, claims 1-3, 5-8 and 10-11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Rejection under 35U.S.C. 112, First Paragraph

The Office Action rejected claims 1 and 6 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Applicants have amended claims and respectfully request for reconsideration of the rejections set forth above.

Discussion of Amendments to the Claims

Applicants have rephrased the terminology of the claims for more clearly and precisely defining the features of the invention. Such amendments including changing "multiplexing finite state machine controller" into "input signal selector", changing "a plurality of registers" into "common storage device" and changing "multiplexer controller" into "output selector." The

amendments comply with the written description of the originally filed specification of the present invention. The claimed subject matters of the amendments are described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. It is also believed that such amendments raise no new matters that again the law.

Discussion of Office Action Rejection by the Crouch

The Office Action rejected claim 1-11 under 35 U.S.C. 102(b), as being anticipated by Crouch. Applicants respectfully traverse the rejections for at least the reasons set forth below.

First of all, Applicants want to emphasize that the Crouch reference relates to "a full scan test architecture." As disclosed in the Col.6, Lines 1-10, it stats that

> "Once the proper scan system is connected or set-up as discussed above, the tester applies **a long serial data vector to the single scan input pin** which is accepted by the flip-flops of the selected functional block to be tested **in a serial manner** while zeros are simultaneously applied to all scan chains in all non-selected functional blocks. While the serial scan vector is being shifted in, the existing state of the scan shift register would be shifted out one bit at a time synchronous to each rising edge of the clock on the single scan output pin, SDO (see FIG. 1).

The Crouch reference does not disclose "sequentially enabling a common storage device to store the test pattern based on a plurality of different states", "after the test pattern is stored in the common storage device, selecting one of the intellectual product circuit modules **according to the test pattern for testing**", "providing the **a test activating signal with a synchronous clock signal** to the selected intellectual product circuit module in a next state", as claimed in claim 1.

The Crouch reference does not disclose an input signal selector to sequentially enable a common storage device to store the test pattern based on a plurality of different states, select one of the intellectual product circuit modules **according to the test pattern for testing** and provides the **a test activating signal with a synchronous clock signal** to the selected intellectual product circuit module in a next state, which are claimed in claim 6.

The Crouch Reference

The test controller 10 of FIG.2 of the Crouch can be explained in Col.7, Lines 54-59, referred to FIG.1, which stated that:

> The test controller 10 will **activate one of the plurality of scan chains by coupling one of the scan chains in the functional blocks 12-22 to the input STDI through the test controller 10**. In addition, the one selected scan chain is coupled through the MUX 24 to the output scan chain which lies between the output of MUX 24 and the SDO pin.

The test controller 10 of the Crouch activates one of the plurality of scan chains by coupling one of the scan chains in the functional blocks 12-22 to the input STDI through the test controller 10. As also stated in the Col.7, Lines 54-59 of the Crouch,

> The logic value applied to the TSTADDR pins when the MTM logic value is set to scan mode, will cause the demultiplexor 40 to connect the scan data in pin 59 to be connected to the first scannable sequential element of the selected partition block.

The Crouch reference disclosed "a full scan test architecture", however, the Crouch reference at least does not disclose an input signal selector to sequentially enable a common storage device to store the test pattern based on a plurality of different states, select one of the intellectual product circuit modules **according to the test pattern for testing** and provides the a

test activating signal with a synchronous clock signal to the selected intellectual product circuit module in a next state.

For at least the foregoing reasons, Applicant respectfully submits that amended claims 1 and 6 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-3, 5, 7-8 and 10-11 are patently defined over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-3, 5-8 and 10-11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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